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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,141	11/13/2003	Budong You	09464-028001	9943

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

HA

Office Action Summary	Application No.	Applicant(s)	
	10/714,141	YOU ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) 1-6 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 7-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Election filed on 11/30/2004.

Currently, claims 1-18 are pending. Claims 1-6 are withdrawn.

Election/Restrictions

1. Applicant's election without traverse of claims 7-18 in the reply filed on 11/30/2004 is acknowledged.

2. Claims 1-6 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected method, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11/30/2004.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 7 -15 are rejected under 35 U.S.C. 103(a) as being obvious over Zuniga et al. (U.S. Patent No. 6,400,126 dated 6/4/2002) in view of Kwon et al. (U.S. Patent No. 6,160,289 dated 12/12/2000).

Zuniga shows the structure substantially as claimed in Figs. 1-6 and corresponding text as: a PMOS transistor (40) connecting the input terminal (20) to an intermediate terminal (22) (col. 3, lines 19-38), the PMOS transistor including a first gate oxide layer (58) (col. 6, lines 18-40); a transistor (42) (NMOS) connecting the intermediate terminal to ground (col. 3, lines 19-38), the transistor including a second gate oxide layer (68) (col. 6, lines 19-40); a controller (18) that drives the PMOS transistor and the transistor to alternately couple the intermediate terminal between the input terminal and ground to generate an intermediate voltage at the intermediate terminal having a rectangular waveform (col. 3, line 55- col. 4, line 4); and a filter (26) disposed between the intermediate terminal and the output terminal (24) to convert the rectangular waveform into a substantially DC voltage at the output terminal (col. 3, lines 39-54) (claim 7). Zuniga teaches that the controller drives the PMOS transistor with a first gate voltage and drives the transistor with a second, different, gate voltage (col. 3, line 55-col. 4, line 4) (claim 8). Zuniga teaches that the second gate voltage is compatible with a CMOS logic circuit (col. 6, lines 41-63) (claim 9). Zuniga teaches that the first gate voltage is larger than the second gate voltage (col. 4, lines 28-36) (claim

10). Zuniga teaches that the second gate oxide layer (68) is thicker than the first gate oxide layer (col. 6, lines 18-40) (claim 11). Zuniga teaches that the PMOS transistor and the transistor have a similar threshold voltage (col. 5, lines 39-53) (claim 12). Zuniga teaches that the PMOS transistor, the transistor, and the controller are monolithically integrated onto a single chip (col. 7, lines 4-18) (claim 13). Zuniga teaches that the controller is fabricated using conventional CMOS transistor (col. 7, lines 4-18) (claim 14).

Zuniga lacks anticipation only in not explicitly teaching that: 1) the transistor of claims 7-14 is an LDMOS transistor; and 2) the PMOS transistor is a p-type LDMOS transistor (claim 15);

Kwon teaches the use of an LDMOS in a Voltage Analog Multiplexer. The high-voltage PMOS transistor (123) which receives the highest voltage V1 and the high voltage NMOS transistor (126) which receives the lowest voltage V4 are made of a mono-directional RESURF LDMOS transistor, respectively (col. 6, line 35-40). The LDMOS transistor is used for high-voltage (10V to 500V) operation, which is compatible with the CMOS VSLI for low voltage (col. 1, lines 23-28). The LDMOS is developed as an element having excellent resistance characteristics for a determined chip size and capable of easily constructing the VLSI (col. 1, lines 29-32).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the structure of Zuniga by replacing the simple NMOS transistor with the LDMOS transistor and that the PMOS transistor is a p-type LDMOS transistor, as taught by Kwon, with the motivation that Kwon teaches that the High-

voltage (10V to 500V) operation, which is compatible with the CMOS VSLI for low voltage and that the LDMOS has excellent resistance characteristics for a determined chip size and capable of easily constructing the VLSI.

7. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuniga et al. (U.S. Patent No. 6,400,126 dated 6/4/2002) in view of Kwon et al. (U.S. Patent No. 6,160,289 dated 12/12/2000) as applied to claim 7 above, and further in view of Grose et al. (U.S. Patent No. 6,384,643 dated 5/7/2002).

Zuniga as modified by Kwon lacks anticipation only in not explicitly teaching that: 1) a PMOS driver to drive the PMOS transistor, and an LDMOS driver to drive the LDMOS transistor (claim 16); 2) the PMOS driver is fabricated using conventional CMOS transistors (claim 17); and 3) the LDMOS driver is fabricated using conventional CMOS transistors (claim 18).

Grose teaches the development of a temperature and process compensated LDMOS drain-source voltage. Grose shows that a PMOS driver is used to drive a PMOS transistor and a LDMOS driver is used to drive a LDMOS transistor (col. 5, lines 56-65). This helps to produce a system that addresses the impacts of and the need for constant drain-source voltage without temperature or process variation (col. 1, lines 47-50).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the structure of Zuniga as modified by Kwon by implementing a conventionally made PMOS driver to drive a PMOS transistor and a conventionally made LDMOS driver to drive a LDMOS transistor as taught by Grose,

with the motivation that Grose teaches the impacts of and the need for constant drain-source voltage without temperature or process variation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WLL
February 17, 2005

MICHAEL S. LEBENTRITT
PRIMARY EXAMINER